

**A PROCESS FOR MANUFACTURING AN INTEGRATED CIRCUIT  
INCLUDING A DUAL-DAMASCENE STRUCTURE AND A CAPACITOR**

**ABSTRACT**

The present invention is directed to a process for forming a dual damascene structure and a capacitor. The process includes forming a stack including insulating layers and a stop layer. The stack is patterned so that the openings used to form the sidewall capacitors may be formed when the vias or grooves of the dual damascene structure is formed. In this way, the process for manufacturing the sidewall capacitors may be integrated with the dual damascene process without adding additional mask or etching steps.

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